REMARKS

The Applicant would like to extend appreciation to the Examiner for allowing claims 2 and 4. By this Response, the Applicant has amended claim 5 and added a new claim 6. The amendment made to claim 5 is fully supported by the specification as originally filed. The new claim 6 is also supported by the specification as originally filed. No new matter has been introduced. Reconsideration of this application as amended, and allowance of all pending claims are hereby respectfully requested.

In the Office Action, claim 5 has been rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,651,224 issued to Sano et al. (hereafter "Sano"). Tha Applicant respectfully traverses the rejection.

Claim 5 is directed to a system that comprises "display means for displaying a reach delay time of each of signals, which reaches a partial circuit on a net list of a gate level". That is, the display means displays a "reach delay time" with respect to each signal and such a displayed "reach delay time" describes a time by which the signal reaches a part of circuit on the net list of a gate level.

Sano discloses a method to optimize signal lines within a circuit (see column 14, lines 12-17, lines 53-59, lines 62-67, Column 15, lines 4-9). Specifically, Sano teaches a method to layout clock signal lines by carrying out clock tree synthesizing processing (see column 14, lines 18-21). Sano discloses four different embodiment of his invention, where the first embodiment is described in FIGs. 1 and 2, the second embodiment in FIGs. 15 and 16, the third embodiment in FIGs. 18 and 19, and the fourth embodiment in FIGs. 21 and 22. Each embodiment includes some different features. For example, compared with the first embodiment depicted in FIG. 1, the second embodiment in FIG. 15 includes an addition "buffer stage number adjustment unit"

547. Similarly, the third embodiment in FIG. 18 includes both an "insert buffer estimating unit" 548 and an "insert buffer selecting unit" 549. However, each of the embodiments has some features that are common to all embodiments. For example, all four embodiments include a display 510 and a display control unit 511 (see FIGs. 1, 15, and 18).

Sano describes the display 510 and the display control unit 511 as being "utilized for displaying various information necessary for synthesizing clock trees or a status of synthesis brought about in the midst of optimization process in terms of clock distribution. In addition, the "display control unit 511 is utilized for controlling display condition of the display 510" (see column 17, lines 39-44). It is clear, according to Sano's disclosure, that the displayed information relates only to clocks, namely clock trees or clock synthesis optimization processes. Sano explicitly states that this is a consistent description across three different embodiments of the invention (see column 26, lines 6-11, column 27, lines 16-18).

As to the fourth embodiment, Sano describes that "the process of determining the LSI layout is composed of a logic design stage S11, a clock layout determining stage S12, and a wiring stage S13" (see column 28, lines 39-46). At each stage, the criterion of the layout is to minimize the wiring length and effective delivery of clock signals to all gates (see column 28, lines 51-67, column 29, lines 1-57). All embodiments are directed to optimizing clock lines among different circuit elements. Information derived from such an optimization process and consequently displayed is information necessary for synthesizing clock trees or a status of synthesis brought about in the midst of optimization process in terms of clock distribution, as stated in Sano (see column 17, lines 39-44). That is, Sano does not teach, disclose, or suggest to either derive information related to "reach delay time" or display "reach delay time", as recited in claim 5.

It is well-settled that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Since Sano fails to disclose and teach the features of "reach delay time" and display thereof, as recited in claim 5, the Applicant respectfully submits that Sano does not anticipate claim 5. Thus, claim 5 is patentable. Therefore, the Applicant respectfully requests that the rejection of claim 5 under 35 U.S.C. §102(e) be withdrawn.

New claim 6 recites the same features "display means for displaying a reach delay time of each of signal, which reaches a partial circuit on a net list of a gate level". Thus, Sano does not anticipate claim 6 for at least the same reasons stated above with respect to claim 5. Therefore, claim 6 is patentable as well.

Accordingly, it is believed that all pending claims are now in condition for allowance. Applicant therefore respectfully requests an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicant's representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF/QH/llg
Facsimile: 202.756.8087
Date: November 22, 2005